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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/633,113
Filing Date: August 01, 2003
Appellant(s): BEUTEN ET AL.

John Lee for Gerard A. Messina
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 7, 2007 appealing from the Office action mailed November 2, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,088,777	Sorber	2000
6,141,756	Bright	2000

6,192,457 Porterfield 2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sorber (6,088,777) in view of Porterfield (6,192,457) and further in view of Bright (6,141,756).

As per claim 1, Sorber discloses a method for providing dynamic memory management of a memory device, the method comprising: providing a first memory block in the memory device [col.3, paragraph 3 and col.5, par.4]; storing a startup program in the first memory block [col.7, par.2]; providing additional memory blocks [col.3, par.2]; and connecting the first memory block and the additional memory blocks by a chained list [col.16, lines 54-57]; wherein the chained list is executed upon checking the memory device [col.7, lines 15-28 and col.8, lines 55-67].

However, Sorber does not specifically teach the startup program obtains data for a check from the additional memory blocks as required by the claim.

Porterfield discloses the startup program obtains data for a check from the additional memory blocks [col.4, lines 3-13] to initialize the computer system upon being turned on (col.4, lines 11-13).

Since the technology for implementing a method for dynamic memory management with the startup program obtaining data for a check from the additional memory blocks was well known as evidenced by Porterfield, an artisan would have been motivated to implement this feature in the system of Sorber since this would have initialized the computer system upon being turned on. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the system of Sorber to include the startup program obtaining data for a check from the additional memory blocks because such feature would have initialized the computer system upon being turned on (col.4, lines 11-13) as taught by Porterfield.

However, Sorber and Porterfield do not explicitly teach the memory device is checked before the chained list is executed as claimed.

Bright discloses a memory device is checked before a chained list is executed [col. 3, ll 15-27] to add security to the bootstrap mode of processors (col. 1, ll 5-7).

Since the technology for implementing a method for dynamic memory management with a memory being checked before a chained list is executed was well

known as evidenced by Bright, an artisan would have been motivated to implement this feature in the system of Sorber and Porterfield in order to add security to the bootstrap mode of processors. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant, to modify the system of Sorber and Porterfield to include a memory being checked before a chained list is executed since this would have helped with adding security to the bootstrap mode of processors (col. 1, ll 5-7) as taught by Bright.

As per claim 2, Sorber discloses the checking is performed using an addition checksum [col.13, lines 10-17].

As per claim 3, Sorber discloses the checking is performed by a cyclic block backup [col.14, lines 5-11].

As per claim 4, Porterfield discloses the checking is performed at a time of booting a system that includes the first memory block and the additional memory blocks [col.4, lines 4-13].

As per claim 5, Porterfield discloses the checking is performed in the background during operation of a system that includes the first memory block and the additional memory blocks [col.4, lines 9-13].

As per claim 6, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 7, Sorber discloses each of the additional memory blocks includes an information area that stores information on the memory block itself [Abstract, lines 17-18].

Porterfield further discloses a checking area that stores information for performing the check [col.4, lines 9-13].

As per claim 8, the rationale in the rejection 1 is herein incorporated. Porterfield further discloses a system, comprising: a computing unit [Fig.1].

As per claim 9, Sorber discloses the memory device includes a non-volatile memory module [col.7, lines 4-7].

As per claim 10, Porterfield discloses the computing unit includes an embedded microcontroller [Fig.1].

As per claim 12, the rationale in the rejection of claim 1 is herein incorporated. Sorber further discloses a computer-readable storage medium including program code for providing dynamic memory management of a memory device, the program code being executable in a computing arrangement [Fig.2].

(10) Response to Argument

Appellant's argument, on page 6, paragraph 1, that "Sorber explicitly indicates that the startup program is contained in the program memory 20, which is separately located from the data memory 22" is clearly erroneous. Appellant further points to Fig. 2 of Sorber in support of his conclusion.

Examiner would like to point out that the "Data Processing and Memory System" of Fig. 2 of Sorber is an Integrated Circuit built on a Single Chip having all the components therein interconnected and functioning as one "Data Processing and Memory System" where all the circuitry and devices are all integrated into and work as one memory system as shown in Fig. 13. Sorber clearly discloses "when memory system 10 is booted up (i.e., startup program loaded from where it is stored in memory) is loaded from and the operating system and other application software are loaded, the memory manager receives a pointer or starting memory address (i.e., a pointer or address of the first location or first block of memory); col. 7, lines 15-25". Additionally, Examiner would also like to point out that there were no specific details in the specification of how any part should be interconnected.

Appellant's argument on page 6, paragraph 2, that Sorber has nothing to do with "storing a startup program in the first memory block...and connecting the first memory block and the additional memory blocks by a chained list" is clearly erroneous.

Examiner respectfully disagrees. Regarding the limitation "connecting a first memory block and the additional memory blocks by a chained list and executing a

chained list", as is well known in the art, a chained list (or linked list) consists of a sequence of nodes (i.e., memory blocks or memory locations), each containing arbitrary data fields and one or two references ("links", pointers) pointing to the next and/or previous nodes (i.e., memory blocks or memory locations). Appellant's remarks filed on August 14, 2006, in response to the rejection of claims 1 and 11-12 under 35 USC 112 first paragraph as failing to comply with the enablement requirement regarding the limitaiton "a chained list is executed", and appellant's submission of US Patent No. 5,249,265 to Liang (Date of Patent: 1993) in refuting the enablement rejection, also attests that "executing a chained list" is very well know in the art .

As shown above, Sorber discloses "storing a startup program in a first memory block; col. 7, lines 15-25". Sorber further discloses in column 16, lines 54-57, "each memory block is linked to a next memory block and a first memory block is indicated by a pointer". Thus. Sorber unequivocally discloses "storing a startup program (i.e., system boot code is loaded) in a first memory block (i.e., thru a memory receiving a pointer or starting memory address)...and connecting the first memory block and the additional memory blocks by a chained list (i.e., each memory block is linked to a next memory block and a first memory block is indicated by a pointer); col. 7, lines 15-25 and col. 16, lines 54-57".

Appellant's argument on page 7, paragraph 3 that "col. 4, lines 3-13 of Porterfield has nothing to do with the startup program obtaining data for a check of the memory

device, which data are obtained from the additional memory blocks" is clearly erroneous.

First of all, Examiner would like to make it clear that the combination of Sorber (6,088,777), Portfield (6,192,457), and Bright (6,141,756) is relied upon for the teaching of the claimed invention. In the final rejection of the claims, Porterfield was relied upon for disclosing "the startup program obtains data for a check from the additional memory blocks". As is evident from Porterfield, col. 4, lines 3-13, "a system address allocation table specifies portions (i.e., blocks) of memory being allocated to set of addresses (example: addresses 0 thru 15M, 15M thru 16M, 16M thru 24M, etc.) and these addresses (i.e., 0 thru 15M, 15M thru 16M, 16M thru 24M, etc.) are used to set the Basic Input-Output System (BIOS) software (i.e., startup program) when the computer system is initialized upon being turned ON" where one of ordinary skill in the art would have recognized and appreciated the function of BIOS (i.e., startup software) in testing or checking system hardware, and BIOS being a set of essential and independent software routines testing system hardware at startup gets data for running any data check from the memory blocks where it is stored thereby avoid corruption (viruses) and maintain authenticity (invalid data) of such essential routines.

Appellant's arguments on page 8, paragraph 3 to page 9 that "there is absolutely no suggestion in Bright regarding any memory device containing the startup program and the additional memory block[s] is checked, let alone that any such memory device is checked before any chained list is executed" are clearly erroneous.

Examiner respectfully disagrees. Claims 1-10 and 12 were finally rejected in an obviousness type rejection using the combination of Sorber, Porterfield, and Bright. Bright, particularly, is relied upon for teaching "a memory device is checked before a chained list is executed". As shown above, a chained list (or linked list) consists of a sequence of nodes (i.e., memory blocks or memory locations), each containing arbitrary data fields and one or two references ("links") pointing to the next and/or previous nodes (i.e., memory blocks or memory locations). Bright clearly discloses "program stored in a memory device has added authenticity information, such as checksum or hash (i.e., checksum and hash are used to implement executable programs using linked/chained lists, a well known practice in software design and implementation), which authenticity information must be authenticated by the processor before the program is executed; col. 3, lines 15-27". Also see remarks filed on August 14, 2006 in response to the rejection of claims 1 and 11-12 under 35 USC 112 first paragraph as failing to comply with the enablement requirement regarding the limitaiton "the chained list is executed". Thus, it is manifest that Bright teaches "authenticity information stored in the memory device (i.e., checksum, hash) must be checked/authenticated before the program (i.e., checksum, hash and codes implemented using linked/chained list) is executed.

Appellant's arguments on page 10 that "there is no logical reason why any person of ordinary skill in the art would be motivated to make the modifications asserted by the Examiner, particularly when one considers the completely different technologies involved in the applied references. There is simply no logical reason why one of ordinary skill in the art would look to these completely unrelated teachings of Sorber, Porterfield and Bright, let alone any reason why one of ordinary skill in the art would specifically combine the selected teachings of these applied reference in the manner asserted by the Examiner" are clearly erroneous.

Examiner would like to point out that, in determining obviousness under 35 U.S.C 103 in view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "By holding that courts and patent examiners should look only to the problem the patentee was trying to solve;" (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem;" (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the conbination of elements was obvious to try;" and (4) by overenphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "[r]igid preventative rules that deny factfinders recourse to common sense."

Furthermore, the Supreme Court stated that: "When a work is available in one field of endeavor, design incentives and other market forces can promp variations of it, either in the same field or a different one. If a technique has been used to improve one

device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the court states that "the focus when making a determination of obviousness should be on what a person of ordianry skill in the pertinent art would have known at the time of the invention...and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowlegdge in the art, or common sense".

Finally, for purposes of 35 U.S.C 103, prior art can be either in the of applicant's endeavor or be reasonably pertinent to the particular problem with which the applicant was concerned. Furthermore, prior art that is in a field of endeavor other than that of the applicant, or solves a problem which is different from that which the applicant was trying to solve, may also be considered for the purposes of 35 U.S.C 103. See, e.g., In re *KSR International Co. v. Teleflex Inc.*, 550 U.S. at_,82 USPQ2d at 1396 (2007).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mardochee Chery
Examiner

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